Please replace paragraph [0021] at page 7 with the following amended paragraph:

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**[0021]** When a sub-instruction reaches the WB stage in block 402, the processor 100 determines whether or not the sub-instruction is the terminal sub-instruction in block 404. For a non-terminal sub-instruction, it is determined whether the result is designated for an architectural register in block 406. If so, the result is written to the SCR 302. If it is determined that the MCI is cancelled in the next cycle in block ~~408~~ 410, the operation 400 ends with the architectural register unaltered by the cancelled MCI. If the MCI is not cancelled, the operation 400 returns to block 402.

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Please replace paragraph [0028] at page 10 with the following amended paragraph:

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**[0028]** According to an embodiment, this problem may be avoided by storing the stack pointer value in the SCR 302 until the Link instruction commits. Referring now to Figure 4, when instruction (3) reaches the WB stage in block 402, it is determined to be a non-terminal sub-instruction in block 404. Since the result is designated for the FPREG, the result, SP, is written to the SCR 302 rather than FPREG. When terminal sub-

instruction (4) reaches the WB stage in block 402, the stack pointer is updated and written to an architectural register reserved for the stack pointer, SPREG, in block 412, and the stack pointer value in the SCR 302 is written to FPREG in block ~~414~~ 416.